AUTOSIR

Surface Insulation Resistance Testing System

GEN3 SYSTEMS

ENGINEERING RELIABILITY IN ELECTRONICS

GEN3 SYSTEMS

Setting the standard
AUTO-SIR™
Surface Insulation Resistance Testing System

The Auto-SIR represents the latest technology in automated precision Surface Insulation Resistance (SIR) testing. The system was developed by Gen3 Systems (formerly Concoat Systems) in collaboration with the world-renowned British, National Physical Laboratory (NPL).

It is currently used for SIR research and test method development by leading research and commercial laboratories around the world.

THE AUTO-SIR TESTS TO:

- IEC 61189-5 (process characterisation)
- ISO 9455-17
- IPC-TM-650
- BELLCORE GR-78-CORE
- DIN GERMAN & JIS JAPANESE STANDARDS

INCLUDING ELEMENTS OF:

- ANSI/IPC-JSTD001C (assembly requirements)
- IPC-JSTD-004 (solder flux characterisation)
- IPC-SM-840 (solder mask)
- IPC-CC-830 & IEC 1086 (conformal coatings)

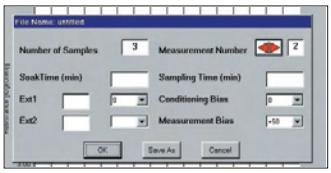
- Gen3 Systems actively co-operates with IEC, ISO, IPC, BSI and other official standards authorities to help maintain and develop measurement standards including SIR testing and long term field reliability materials and process characterisation protocols.
- The Auto-SIR performs SIR testing in accordance with all major international standards (above) via a comprehensive range of standard and optional features (see opposite).

Key features include:

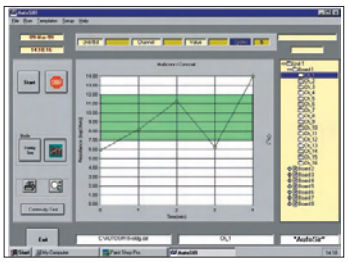
- FMTA Automatic frequent monitoring
- Configurable from 1 up to 64 or 256 sites (Auto-SIR 64 and 256 units respectively) and expandable up to 2048 maximum
- Standard programmable bias voltages of ±50 V and ±100 V, plus non-standard voltages via an external power supply
- 1 MΩ current limiting resistors to preserve dendrite formations for subsequent failure analysis
- 3 to 500 V selectable measurement voltages
- Power supplies for higher bias and measurement voltages available
- Input and switching control for external power supply up to 500 V
- Accessories include: pre-wired test racks, test kit, cables, and connector harnesses
- CD-ROM instruction and system operation manual

AUTO-SIR Windows® software is designed for repetitive SIR testing to all major test standards

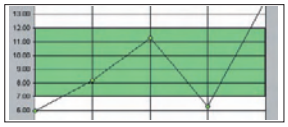
- All SIR test parameters are fully selectable in the software
- Data logging test intervals are fully selectable as defined by the particular test specification in use



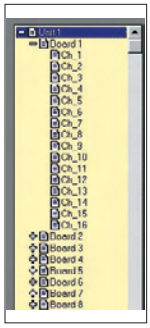
- Each test channel can be viewed selectively as a single graph. The individual status of each single channel can be printed at any stage of the test



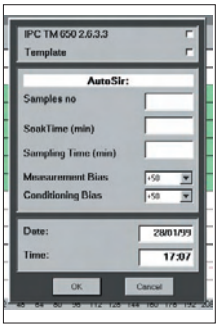
- Selecting an individual plotted data point and right clicking will display the associated time and resistance



- Graph zoom function for easier viewing
- The 32-bit software reads long file names so each data file can have a unique user name and is date stamped for easy retrieval



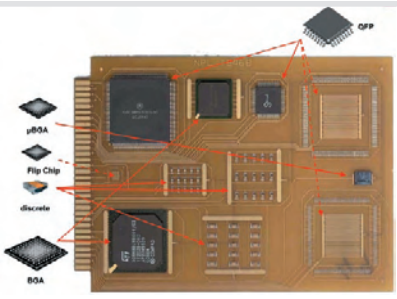
- Standard test templates according to all international standards are part of the software
- User definable templates are easy to configure and re-use. Flexibility allows future test parameters to be defined



- All output data is in a delimited data file that can be exported to any spreadsheet software for further evaluation or analysis
- Optional temperature/humidity chamber monitoring – including SIR graphing

NEW: ***PROCESS CHARACTERISATION TEST KIT COMPRISING:***

- **Test vehicle Gerber file**
- **Full set of SIR dummy components**



Example of completed IEC 61189-5 test vehicle

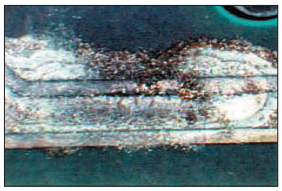
Basic Principles of SIR Testing

"SIR testing is a methodology used to evaluate electronic assembly materials and processes as one measure of reliability. The goal of SIR testing is to catch dangerous propensities for electrochemical failure mechanisms, such as unacceptable electrical leakage under humid conditions, corrosion or metal migration, before they can occur on produced assemblies."

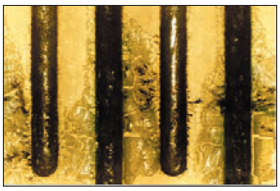
Douglas O Pauls: IPC Technical Activities Executive, Chairman of IPC Cleaning & Coating Committee & Senior Process Engineer, Rockwell Collins

Three factors need to be present for electrochemical failure to occur: electrical potential, moisture and an ionic residue. Electrochemical failure can best be visualised using the Venn diagram shown below. Increasing and decreasing these factors can be thought of as increasing and decreasing the diameter of the circles.

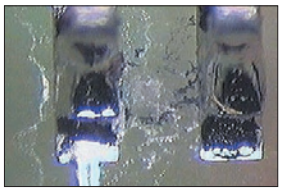
In SIR testing, temperature and humidity levels are artificially elevated to accelerate the moisture factor. A voltage is applied to provide a power source. If the test substrate has a low ionic content, then the measured SIR will remain 'acceptable'. If the ionic content is high, such as from improperly cured solder resist or from flux residues, then 'unacceptable' leakage currents, corrosion and metal migration, or dendritic growth will occur. Each SIR test method, standard or specification defines what is 'acceptable' and 'unacceptable'.



corrosion

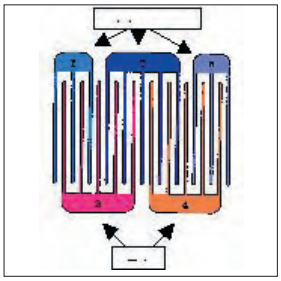


dendritic growth

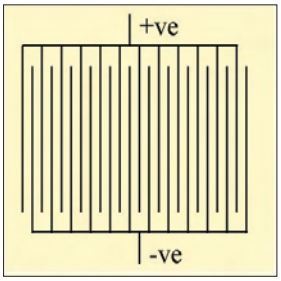


metal migration

dendrite in detail

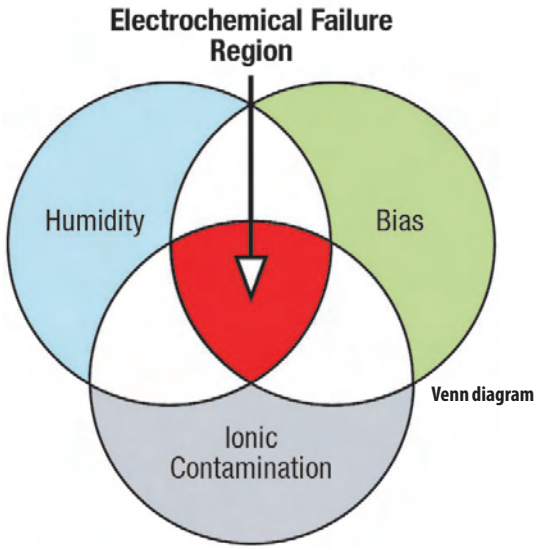


'Old' Bellcore 5-point test pattern

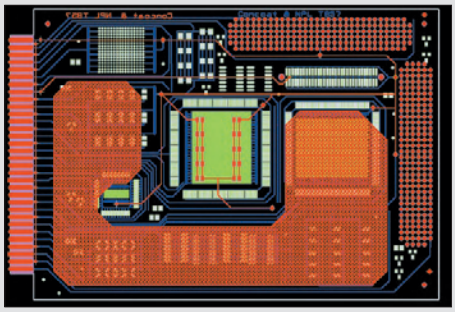


'New' IPC/IEC inter-digitated pattern

SIR testing is usually performed on industry standard test board coupons containing patterns, typically interdigitated combs, designed for the purpose. The insulation resistance of a test pattern is monitored at various intervals as temperature and humidity are varied. Monitored resistance levels may range from 10^6 to 10^{14} Log Ω. Test specifications can call for several different types of test coupons and test conditions as illustrated in Table 1.



Venn diagram



A Gerber schematic of the Gen3 Systems/NPL TB57 process characterisation test vehicle from which both the IEC and IPC test coupons are derived.

How test pattern, coupon & voltage affect SIR

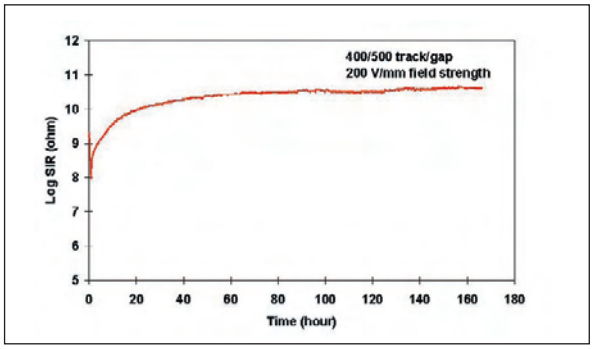
TEST PATTERN AND COUPON

It is generally recognised that SIR data is dependent on the geometry and design of the SIR test pattern. Recent research by the NPL has shown that pattern geometry differences can cause up to a decade difference in measured results.

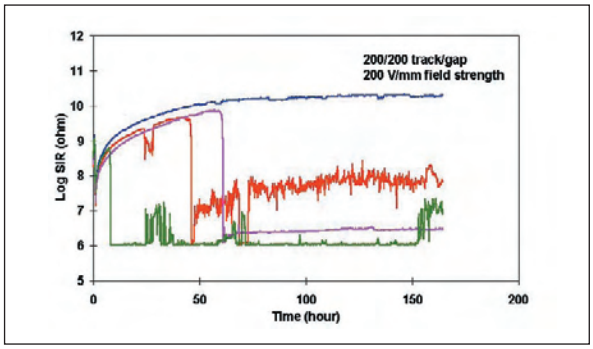
When running process evaluations, it is important to choose the same mix of materials in the test coupon and pattern as found in the hardware to be produced (e.g. laminate/mask/metal).

If the SIR test pattern incorporates component mounting pads, then it is critical that the components mounted on these pads have NO internal connections. Typical dummy components contain blown dies internal to the package and are unsuitable for SIR testing.

If SIR patterns are being designed, the ends of each conductor should be rounded to avoid sharp discontinuities where electromigration can initiate. In addition, a well designed test pattern will have guard/ground traces to completely isolate power lines from ground planes.



400/500 Track/Gap 200 V/mm



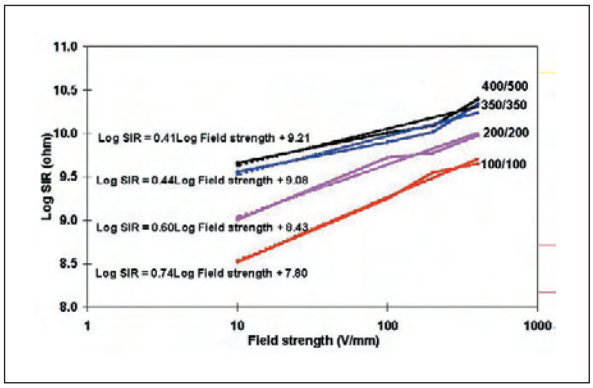
200/200 Track/Gap 200 V/mm

VOLTAGE GRADIENT (FIELD STRENGTH)

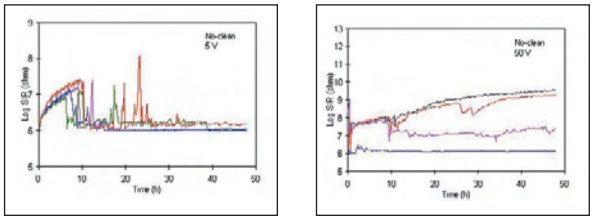
The voltage gradient is the applied voltage level divided by the spacing between the conductors, usually expressed in volts per mm (V/mm). Most test methods specify the voltage to be applied, but this voltage may be applied to patterns with different conductor spaces, leading to multiple voltage gradients on the same test substrate.

An example is the IPC-B-36 test board in which a 50 V bias is applied to the test pattern. Some patterns have a 0.15 mm spacing (333 V/mm) and others have a 0.64 mm spacing (78 V/mm). Some test methods also specify reversing voltage polarity between bias and measurement phases.

Recent research has indicated an optimum voltage gradient of 25 V/mm, with no reverse polarity and lower bias/measure voltages (5 V) for SIR testing. This research has also found that SIR testing does not precisely obey Ohm's Law and it is therefore important that any new characterisation testing take this issue into account.



Field strength vs pattern design



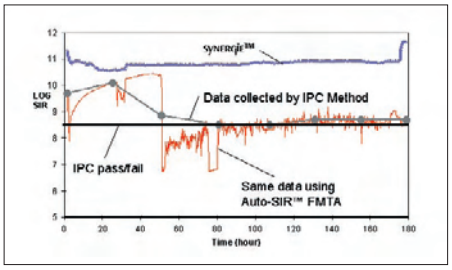
Auto-SIR test graphs showing 4 individual test sites and the influence of test voltage on dendrite formations

All graphs courtesy of NPL and the EU Collaborative SIR Research Programme.

Test intervals

Most current SIR test methods evolved from manual measurement techniques and so have infrequent measurement intervals, such as 24 hours. It has been shown in many cases that electromechanical failures can occur frequently between measurement intervals, often leaving no trace that a failure event has occurred.

Therefore, the more frequent the measurement, the greater the probability of catching failures. In addition, if the measurement pathway contains current limiting resistors (e.g. 1 MΩ), a dendrite is usually preserved for detection in post-test visual examination. The Auto-SIR can be programmed with measurement intervals as low as 5 minutes and as great as 7 days.



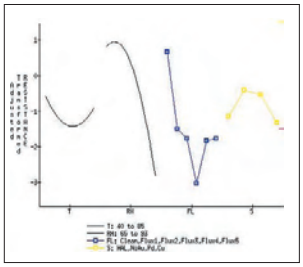
The long test intervals of prevailing standards (grey line IPC-TM-650) can completely miss the frequent formation and collapse of dendrites (red line taken using Auto-SIR FMTA)

Test environment

SIR levels generally decrease as temperature and humidity increase due to the formation of monolayers of moisture on the test surface. The addition of ionic material to the moisture, either from the substrate or surface residues, will further reduce SIR levels. Temperature and humidity levels vary greatly between different specifications, dependent upon the test goals.

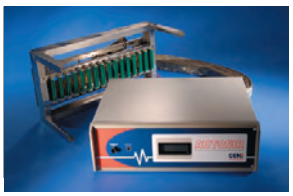
Some specifications simulate end-use conditions, others accelerate electromechanical failure mechanisms, such as leakage currents, corrosion, and metal migration. The selection of the test environment is a critical factor in materials/process evaluations. Research shows that lower test temperatures (e.g. 40 °C) are a more stringent test for easily volatilised residues such as low residue fluxes.

For process characterisation (such as the IEC 61189-5 specification) the test temperature and humidity should reflect typical anticipated operating conditions for the end product.



EU SIR programme results showing relative SIR influences of temperature, relative humidity, flux and surface finish (NMRC)

How the **AUTO-SIR** works



The Gen3 Systems Auto-SIR system represents a dramatic improvement over existing SIR test alternatives, and its shielded precision electronics allows state-of-the-art accuracy resistance measurements to be made up to 10^{14} Log Ω.

One Auto-SIR chassis can hold between 1 to 16 measurement cards and can monitor up to 256 x 2-point test patterns or 80 x 5-point test patterns, at selectable intervals from minutes to days. Auto-SIR units can be daisy-chained together for greater capacity, if desired. Each channel is current limited (1 M Ω), ensuring that dendrites are preserved for failure analysis. The frequent monitoring capability provides a full picture of the electrochemical reactions taking place on a circuit assembly, and provides early trend analysis enabling tests to be curtailed, thus saving considerable test time and money.

A unique feature of the Auto-SIR system is Frequent Monitoring Trend Analysis (FMTA). This methodology is used to examine SIR trends over time, primarily to detect in-situ dendritic growth at each 'wet process' manufacturing stage. Gen3 Systems has also developed an extended software package to make measurements within the environmental chamber. This optional independent temperature-humidity monitoring records the environmental conditions next to the coupon under test, as the data is gathered, for more accurate data analysis.

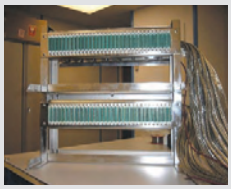
All cabling in the Auto-SIR is PTFE insulated with wires shielded from EMI. The design of the data acquisition cards minimises channel-to-channel leakage. This is important because the extremely low levels of current involved in SIR measurement means any stray currents (including electromagnetic noise or leakage between wire insulations) can significantly affect measurement accuracy.

The Auto-SIR instrument is delivered complete with:

- **Auto-SIR 64 instrument (expandable in increments of 64 channels to a maximum of 256)**
- **Operating software**
- **ALL interconnecting cables (screened halogen-free)**
- **Optional test racks simplify SIR testing and reduce test time and test costs.**

IMPORTANT NOTE: Test racks are coupon specific

Test coupons in test rack



Auto-SIR test rack

Test Standards & Methods

Table 1

STANDARD	IEC 61189-5	ISO 9455-17	J-STD-001C	IPC-TM-650	IPC-TM-650 2.6.3	Bellcore 2.6.3.3
Temperature/ Humidity	40°C/93% RH (No Clean) 85°C/85% RH (Clean)	85°C/85% RH	85°C/85% RH	Class 1 - 35/90°C at 98% RH for 4 days static Class 2 - 50/90°C at 98% RH for 7 days static Class 3 - 25/65°C at 90/98% RH for 7 days cycling	85°C/85% RH	35°C/85% RH
Test Duration	Not less than 72 Hours	168 Hours	168 Hours	168 Hours	168 Hours	120 Hours
Measurement Frequency	Measured at 20min intervals	Measured twice a day	Measured at 24hrs, 94hrs and 168hrs	Measured at 24hr intervals	Measured at 24hrs, 94hrs and 168hrs	Measured at 25hrs and 120hrs
Test voltage Bias	5V +5V	50V +50V	100V –50V	100V –50V	100V –50V	100V –50V
Test Coupon	IPC-B-52	IPC-B-24	IPC-B-36	IPC-B-25A	IPC-B-24	IPC-B-25A

The Table above illustrates how greatly the requirements of the most common SIR test standards vary in terms of duration of the test, the applied voltages, the measurement frequency, the temperature and humidity levels used and the acceptance criteria.

Due to the extremely low currents involved, SIR testing has several critical factors in reaching accurate conclusions. It is recommended that reference be made to 'IPC-9201 The SIR Handbook' for further detailed guidance on the subject.

Gen3's technical personnel have taken an active and continuing part in the development of modern ISO, IEC and ANSI/IPC SIR test methods, standards and specifications.

The Auto-SIR was developed in conjunction with industry technical experts, as well as major research and commercial test laboratories, to accurately accommodate all current SIR test methods, as well as anticipate future SIR test method evolution.

PROCESS CHARACTERISATION TESTING

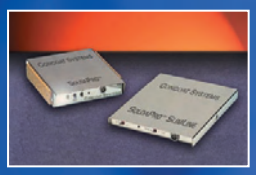
When running process evaluations, the selection of the materials for SIR testing has a major impact on the end result. If a materials characterisation test is being performed, such as flux evaluations per ANSI J-STD-004, then the laminate and metalisation is fixed (FR4 and bare copper, respectively) in order to provide a consistent evaluation platform.

If SIR testing is used as part of an engineering process evaluation, however, it is important to choose the same mix of materials in the test coupon and pattern as found in the hardware to be produced (e.g. laminate, solder resist, metalisation, flux, paste, adhesive, coating, etc.). Gen3 Systems can also supply a process characterisation test kit.

TECHNICAL SPECIFICATION

TEST VOLTAGE:	5 V, 10 V, 50 V, 100 V – OR WITH EXTERNAL P.S. UP TO 500 V
BIAS VOLTAGE:	5 V, 10 V, 50 V, 100 V, –50 V, –100 V – OR WITH EXTERNAL P.S. UP TO 500 V
MEASUREMENT RANGE:	10^6 LOG Ω TO 10^{13} LOG Ω
SYSTEM TOLERANCE AS PER IEC 61189-5 (I.E. TOTAL MEASUREMENT SYSTEM):	
	UP TO 10^{10} LOG Ω ± 5 %
	FROM 10^{10} LOG Ω TO 10^{11} LOG Ω ± 10 %
	ABOVE 10^{11} LOG Ω ± 20 %
LOGGING FREQUENCY:	EVERY 20 MINUTES
TEST CABLES:	SCREENED HALOGEN-FREE
POWER SUPPLY:	240 V, 50 Hz or 110 V, 60 Hz
SOFTWARE FOR WINDOWS 98, NT & XP	AUTO-SIR FMTA TESTING (STANDARD)
	BELLCORE TESTING (OPTIONAL)
	IPC B25A TESTING (OPTIONAL)
CONTROL INTERFACE:	RS 232
COMPUTER REQUIREMENTS (MINIMUM) – NOT REQUIRED FOR RACK UNIT:	
PENTIUM III, 256 MBYTE RAM, HDD PRIMARY & SLAVE, SERIAL PORT, WINDOWS 98, NT OR XP OPERATING SYSTEM	

MUST SYSTEM 3
SOLDERABILITY TESTING SYSTEM



SOLDAPRO
THERMAL PROFILING

AUTO-SIR
SURFACE INSULATION RESISTANCE TESTING

CM-SERIES
CONTAMINATION TESTING

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